Overview

The Physical Coding Sublayer (PCS) IP Core enables transmission and reception of data via 8-Lanes SerDes interface. It is able to multiplex a synchronous digital stream of data over 8 Lanes, while guaranteeing data alignment and super-frame synchronization. The PCS is responsible for idle sequence generation, lane striping and encoding for transmission and decoding, lane alignment and restriping on reception. The PCS uses an 8B/10B encoding for transmission over the link.

This IP core has been designed and verified using Cadence state-of-the-art EDA tools, methodology and recommended design and verification flow.

External Interfaces

APB interface: APB interface is used for configuration of PCS IP core. It is compatible with AMBA APBv1.0. It allows external access to core’s (and Ser/Des) configuration, status and error counters.

SerDes interface: This interface is used to transfer/receive 10-bit data to Ser/from Des. It provides 10-bit clock for Ser/Des and contains a number of signals used for Ser/Des configuration. Data interface: Parallel interface through which PCS IP receives super frames to be processed and through which PCS delivers reconstructed frames received from Des Lanes.

Blocks description

REG_FILE: holds configuration and status registers.
CLK_DIV: Clock divider which divides functional clock and provides referent clock for Ser/Des Lane’s PLLs.
SF_GEN: This is a Super Frame (SF) generation module which takes an incoming stream of data from the ILB block, and packs it into SF structure (eight 8-bits output data streams) that are ready to be encoded. Each Super Frame starts with Lane Marker character that is transmitted over all 8 Lanes. In case when there is no SF on its input, SF_GEN is responsible for insertion of idle characters.

8B10B_ENC: The 8B10B encoder converts payload and control octets into 10 bit words. There are 8 instances of this block, one per lane, denoted 8B10B_ENC0 – 8B10B_ENC7. The usage of 8B10B code improves the transmission characteristics of information to be transferred across the link. It ensures that sufficient transitions are present in the PHY bit stream to make clock recovery possible at the receiver. The encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during reception of information.

SF_REC: This module performs the super frame recovery function, and unpacks the data stream received from the 8 channels into a data output bus. It contains lane alignment logic which compensates for the skew accommodated by each lane. SF_REC ignores idle characters; it starts to reconstruct frames upon detection of lane marker character.
8B10B_DEC: This block first performs the framing functionality, aligns the bit-stream received from the Des to 8B10B block boundaries. The second function of this block is 10B8B decoding, conversion of 10-bit code words into 8 bit words. There are 8 instances of this block, one per lane, denoted 8B10B_DEC0 – 8B10B_DEC7.

ELB: The external-facing loopback block (ELB) provides per-lane loopback, and per-lane PRBS generation and verification functionality. PRBS polynomial used is PRBS31: 1+x^28+x^31. In case when neither PRBS nor Loopback is enabled the ELB is transparent for data generated by SF_GEN/8B10B_DEC.

ILB: The internal-facing loopback block (ILB) provides PRBS generation and verification on the payload, including super-frame alignment and verification of the PRBS sequence. PRBS polynomial used here is PRBS31: 1+x^28+x^31. In case when PRBS is not enabled, the ILB block is transparent for SF_REC data or data received on RX Data interface.

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Contact Information

HDL Design House
Golsvortijeva 35,
Belgrade, Serbia
Phone: +381 11 414 55 55
Fax: +381 11 414 55 59
Email: info@hdl-dh.com
http://www.hdl-dh.com

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