HIP 3700 I2S Soft IP core

01.10.2009.

Design House
SoC Design and Verification Company

The use of IP cores in ASIC, FGPA and system-on-chip (SoC) designs has become a critical methodology as companies struggle to address the need for rapid prototyping and production. Reusable, drop-in components with predefined functionality, IP cores speed the design cycle, increase design quality and allow a greater degree of innovation, enabling companies to reduce design costs and create market differentiation.

HDL Design House provides a set of IP cores for reuse along with IP core customization services to meet specific customer needs. Optimized for today's SoC designs, these IP cores are supported with full documentation, including architectural and micro-architectural specifications, synthesis scripts, detailed test plans, test case definitions and test bench descriptions.
This IP core has been designed and verified using Cadence state-of-the-art EDA tools, methodology and recommended design and verification flow.

I2S IP Core (HIP 3700)

I2S is an audio transmission standard, used to connect system elements such as Analog to Digital and Digital to Analog converters, speakers or audio subsystems. HIP 3700 is silicon proven I2S Controller IP Core compliant to the Philips* Inter-IC Sound specification. IP Core provides up to 8 audio channels and a 32-bit parallel processor bus as the application interface. Each channel can be programmed as an I2S master or an I2S slave.

Key Features:

- *IP core meets the Philips Inter-IC Sound bus specification*
- *Supports configurable 8/16/24/32 bit DAC/ADC resolution*
- *Supports Master/Slave and Receiver/Transmitter modes*
- *Two sets of SCK (SCLK) and WS strobes:*
  - *One for all transmitters*
  - *One for all receivers*
- *32-bit parallel AMBA APB processor bus (other custom specific buses can also be provided upon request).*
- *Configurable internal FIFO's (one for all transmitter channels and one for all receiver channels)*
- *Audio sampling capabilities:8, 16, 24, 32, 44.1, 48; 88.2; 96; 176.4; 192kHz*
- *The I2S Bus Interface may operate in one of the following four configurations:*
  - *I2S – Philips mode*
  - *Left Justified mode*
  - *Right Justified mode*
  - *DSP mode*
- *Mode of operation for each channel can be set in the single configuration register*
- *IRQ driven by the I2S bus events*

Applications

The I2S IP core can be utilized for a variety of Inter-IC Sound compliant serial bus applications:

- ASIC and SoC applications requiring up to 8 channel audio data transmission
- Digital signal processing and multimedia systems
- Connecting Analog to Digital and Digital to Analog converters
- Digital audio interface of embedded microcontroller systems

HDL Design House, Golsvortijeva 35, Belgrade, Serbia
Phone: +381 11 414 55 55 Fax: +381 414 55 59 Email: info@hdl-dh.com On-line: http://www.hdl-dh.com

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Deliverables

- Verilog RTL source code
- Functional specification
- Microarchitecture specification with detailed core integration guide

Benefits:

- *User configurable formaximumflexibility*
- *Easy to integrate into complex SoC designs*
- *Shortens development cycles*
- *Speeds time tomarket of new products*
- *Enables innovation andmarket differentiation*

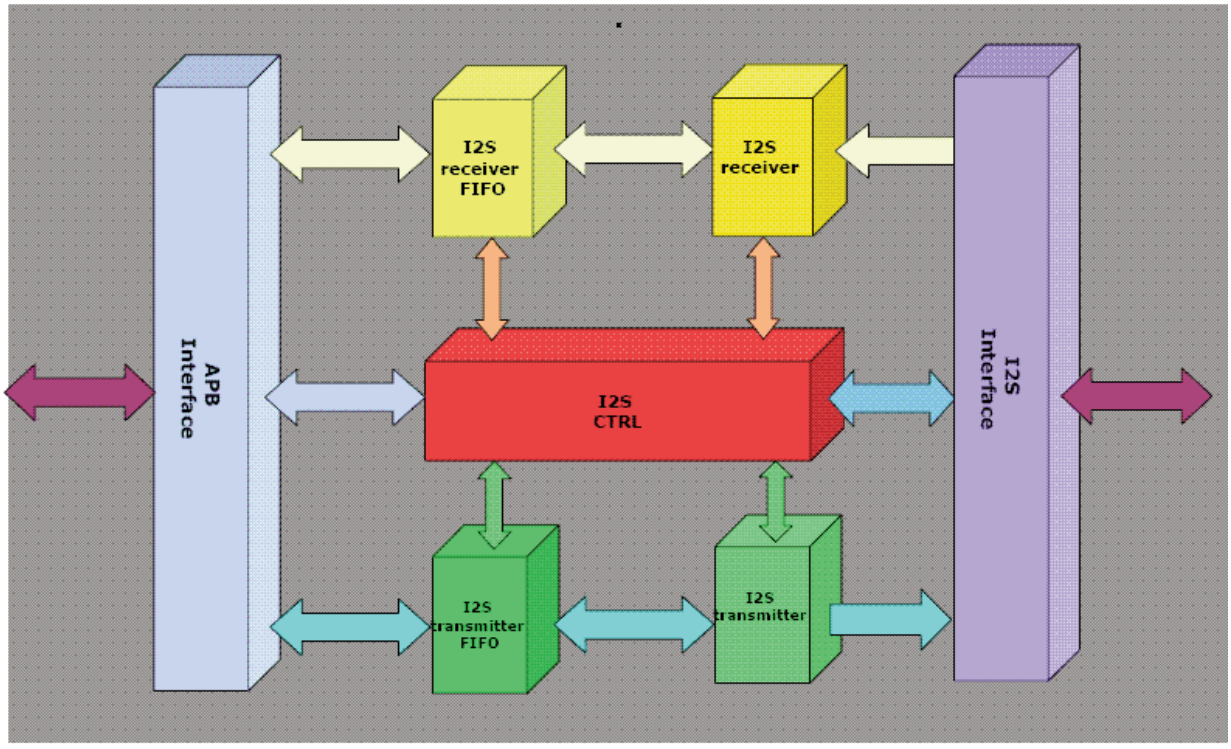

Figure1. HIP 3700 I2S block level diagram

HDL Design House, Golsvortijeva 35, Belgrade, Serbia
Phone: +381 11 414 55 55 Fax: +381 414 55 59 Email: info@hdl-dh.com On-line: http://www.hdl-dh.com

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IP core overview

IP core design is strictly synchronous with two clock domains. Positive-edge clocking is in both domains. There are no internal tree-states and asynchronous resets, therefore scan insertion is straightforward. The I2S engine requires an external master clock input. Single I2S channel uses three wires to transfer information between devices connected to the bus: SCK (continuous serial clock), WS (word select) and SD (serial data).

The bus has to handle only audio data, while other signals (control) are transferred separately. Audio data coming from two channels is time-multiplexed to the single line SD. Left channel data is transmitted when WS = 0, while right channel data is transmitted if WS = 1. Serial data is transmitted in two's complement with the MSB first.

The transmitter always sends the MSB of the next word one clock period after WS changes. This input (MCLK) is used to generate the SCLK, WS , SD, and drive the internal logic of the I2S engine. The MCLK is also used to directly drive the SCLK output. The WS signal is toggled at a rate of MCLK / 512 allowing all standard sampling frequencies to be achieved with the appropriate MCLK frequency. The core has been tested in simulation with behavioral model of Texas Instruments PCM1742 DAC.

HDL Design House Representatives

For complete list of HDL Design House representatives visit following link:
http://www.hdl-dh.com/sales_rep.html

Contact Information

HDL Design House
Golsvortijeva 35,
Belgrade, Serbia
Phone: +381 11 414 55 55
Fax: +381 11 414 55 59
Email: info@hdl-dh.com
http://www.hdl-dh.com