# HIP 3600 UniPro IP Core

03.06.2011.

Design House
SoC Design and Verification Company

## HIP3600 IP Core Overview

UniPro is a high speed interface technology for interconnecting devices and integrated circuits within mobile systems such as cellular phones, handheld computers, and other multimedia devices or comparable products. The structural and layered interfaces of UniPro allow these mobile devices and components for high-speed data communication, low power per transferred bit and low pin counts without sacrificing data reliability and robustness.

HDL DH's UniPro IP core (HIP3600 ) complies with the MIPI UniPro specification v-1.4 r0-12. HIP3600 implements the Physical-Adapter Layer (L.15), Data Link Layer (L2), Network Layer (L3) and Transport Layer (L4). It is compatible with both D-PHY and the M-PHY Physical Layer . HIP3600 exhibits a complete set of components using AMBA's AHB and AXI Version 2.0.

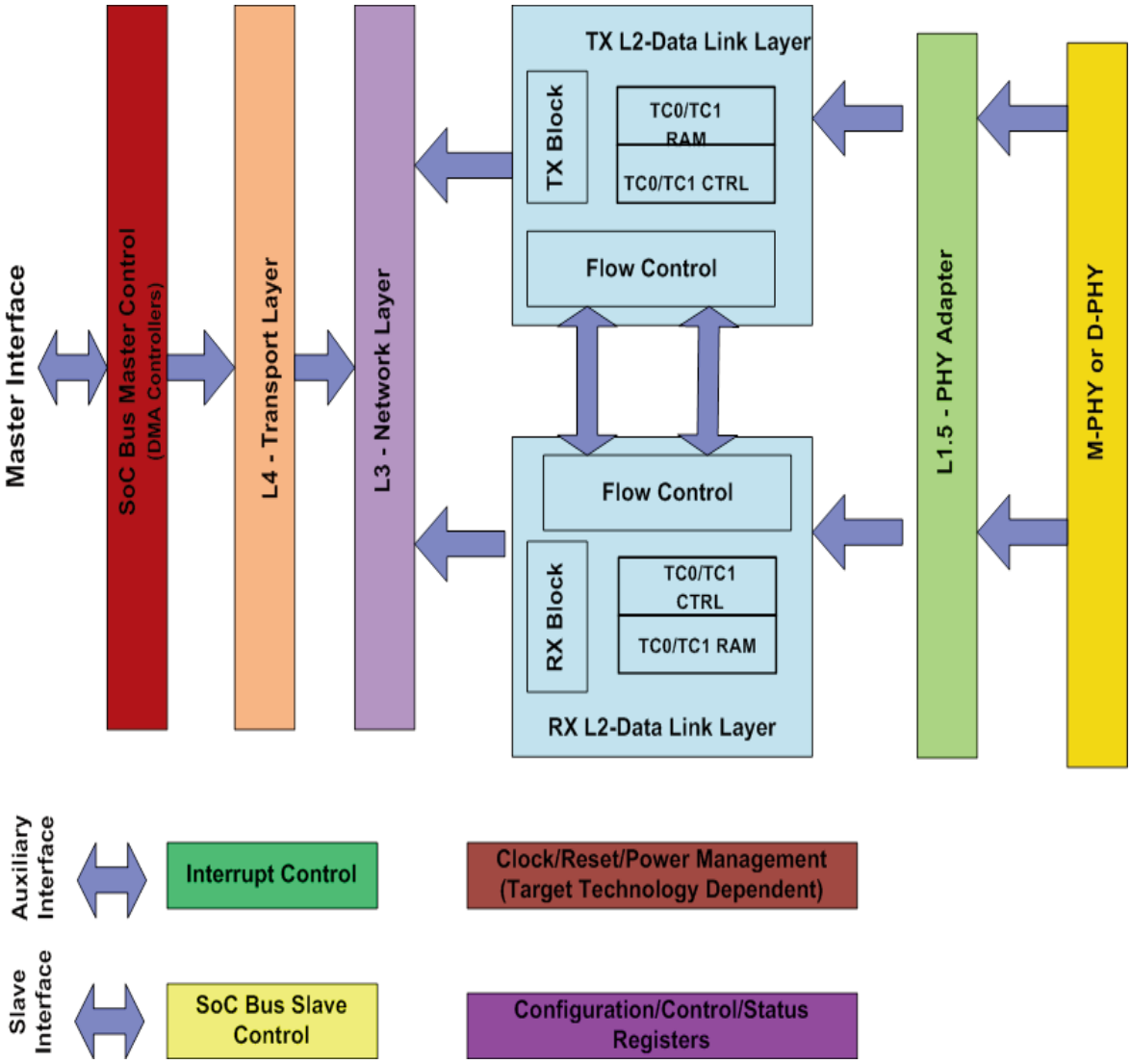


***Figure1. HIP 3600 UniPro block level diagram***



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## System Interface

One SoC Bus Master interface is provided for high speed data transfer to the system memory, and one SoC Bus Slave interface is used for access to the 32-bit configuration registers. The bus master interface can operate at a maximum frequency of 266 MHz to sustain the maximum throughput of 2 GByte/sec. The bus protocols supported by default are AMBA AHB and AXI or OCP depending on the request of the customer.

## The Transport and Network Layers

The Transport Layer of the HIP3600 has a software configurable number of CPORTs, which can accommodate up to 2048 ports. End to End flow control via a credit based scheme is supported, as well as the implementation of the Controlled Segment Dropping and Control Safety Valve features.

The Network Layer handles 2 traffic classes (TC0 and TC1) with prioritization of TC1. It supports both short and long header packets.

## The Data Link Layer

The Data Link layer's transmit and receive blocks implements Data Link Layer protocol features of the UniPro 1.4. standard. The transmit block is enabled when data transfer requests are received from the upper layer, and moves data from the replay buffer to the PHY Adapter layer. The replay buffer can store a maximum of 16 frames for each traffic class until they are acknowledged by the peer. The receive block analyzes the data stream coming from the PHY Adapter by extracting the raw data payload from the stream and performing integrity checks on-the-fly. It also informs the upper layer when an error free data is completely received.

## PHY Adapter Layer

This block implements the PHY Adapter Layer protocol of the UniPro standard. It receives frames from the Data Link Layer and splits them across connected PHY. On reception, it merges symbols received from the M-PHY or D-PHY into symbol stream. This stream is forwarded to the Data Link Layer of the IP Core. PHY Adapter layer also handles insertion/detection of PHY Adapter Control Protocol (PACP) Frames. PHY Adapter has support to access/configure PHY attributes via separate interface.

## Other Blocks

The interrupt control has a minimum of two interrupt lines to support normal and high priority asynchronous event notification to the on-chip processors. Additional interrupt lines can be added in HIP3600 to support multiple levels of interrupt priorities. Interrupts can be used to send asynchronous notifications to the system firmware about the status of the data frame transfers or about the errors detected within the different layers of UniPro.



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**Feature Summaries:**

- Bus Interface
- AMBA AHB Verson 2.0 Compliant Slave Interface
- AMBA AXI Version 2.0 Compliant Master Interface
- Customized interfaces can also be supported on request

**Generic Features:**

- Compliant to MIPI UniPro Specification v-1.40 r0-12
- Support for up to 2048 independent CPorts or logical connections
- End-to-End flow control, Controlled Segment Dropping (CSD) and CPort Safety Valve (CSV)
- Long Header (L3s=0) Trap
- Up to 2 Traffic Classes
- Built-in Test Features (in both L4 and L1.5)
- Built-in DMA Controller
- Implements 6 DMA channels, two channles dedicated for fethcing and flushing of descriptors and four channels shared between read and write data transfer
- Support for preemption of low priority data frames by higher priority traffic class
- Detection of preempted frame on the receiver
- DL Layer flow control to prevent overflow of receiver buffer
- Error detection mechanism for preventing deadlock situations
- Autonomous error detection, error handling, and error recovery in DL Layer
- Remote UniPro Attribute access
- Interrupt Reporting
- Power management modes (customer specific requirements)
- Supports M-PHY and D-PHY Protocol Interface
- Fully synchronous design
- Available in synthesizable Verilog hardware description language
- Possibility of using different kind of memories with configurable size

## Deliverables

- Verilog RTL source code
- Comprehensive documentation package
- Functional specification
- Microarchitecture
- User guide



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This IP core has been designed and verified using Cadence state-of-the-art EDA tools, methodology and recommended design and verification flow:

## HDL Design House Representatives

For complete list of HDL Design House representatives visit following link:
**http://www.hdl-dh.com/sales_rep.html**

## Contact Information

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