Serial RapidIO is a data communication standard provisioned for the interconnection of devices on the same circuit board or between circuit boards across a backplane. It has been developed as a more cost-effective, standards, switched based replacement for expensive proprietary buses in high-performance embedded systems, such as networking and communications equipment and enterprise storage. HIP 3300 Serial RapidIO endpoint soft IP core is based around a generic, modular architecture from which a variety of solutions can be easily created to effectively and efficiently address customers’ specific requirements. The HIP 3300 Serial RapidIO IP solution is a complete high-performance core that incorporates a logical layer, a transport layer, and a physical layer according to the RapidIO specification ver 2.1. HIP3300 IP core also supports I/O and message-passing. The core provides a Serial RapidIO interface on one side and ARM’s AMBA 3 AHB, high performance interface on the other side of the core, allowing flexible and high performance communication with host CPU. Modular design of the IP core allows easy implementation of add-on third party bus interfaces and/or other standard bus interface. IP core also has internal multi-channel DMA descriptor based, controller that fully exploits AHB protocol features and thus supports highest available data throughput and back to back packet transmissions.

Key Features:
- Conforms to the latest RapidIO Interconnect specification – Rev.2.1
- AMBA 3 AHB ARM CPU host interface, for high performance on-chip communication.
- Supports multiple high speed lanes, (1x, 2x, 4x, 8x and 16x modes)
- Configurable modes of operation; 1.25 Gbaud/s, 2.5 Gbaud/s, 3.125 Gbaud/s, 5Gbaud/s, 6.25Gbaud/s transfer rates
- Internal multi-channel DMA, descriptor based, controller that fully exploits AHB protocol features and thus supports highest available data throughput and back to back packets transmission.
- Configuration and Status Register File containing over 40 architectural registers providing total software control of IP core.
- Number of software maskable interrupt request signals.
- Full backward compatibility with RapidIO specification revision 1.3
- Provides roadmap to future RapidIO specification revisions.
- IP core version with AMBA AXI interface is option

Benefits:
- Highly Configurable
- Modularized for IP reuse
- Fully synchronous
- Clearly defined clock domains
- Layered architecture
HIP 3300 IP Core Overview

HIP 3300 IP Core consist of following main blocks:

**AHB master interface (32/64 bits).** AHB master is used in cooperation with DMA engine as support for Packet payload copy to/from Host memory. It is active if DMA operation is enabled, only. It will initiate both read and write AHB access. AHB interconnection approach is shared address buses and multiple data buses.

**AHB slave interface (32/64 bits).** It will provide Host read/write access to Control and Status register set and thus provides a mean for SW to initiate or inspect SRLIO transaction.

![Figure 1. HIP 3300 IP Core Block Diagram](image-url)
Interface will support wait states insertion and burst access. AHB interconnection approach is shared address buses and multiple data buses.

**DMA engine.** Multi-channel descriptor based DMA controls block transfers to/from Host memory using AHB master interface. Used as run-time option can be enabled or disabled for specific types of SRIO transaction asserting appropriate CSR bit Main purpose of DMA engine is to decrease CPU overhead related to Packet payload transfer to/from Host memory. Burst transfers on AHB bus improves overall performance of system (Host-Core).

**Configuration and Status registers.** There will be one set of configuration registers for HIP 3300 Core (general configuration parameters) and Serial RapidIO standard specific register file. Core specific CSR contains storage for all necessary Serial RapidIO packet fields. SW can initiates (for TX Packets) or inspect (for RX Packet) CSR registers and thus control traffic.

**TX Packet processor.** This block performs Serial RapidIO packet composition and delivery to Physical layer. Host provides packet content initializing CSR registers.

**RX packet processor.** This block extract Serial RapidIO packet fields from Physical layer data stream and update corresponding CSR registers. Host is able to inspect Serial RapidIO events by CSR.

**Packet protection.** Serial RapidIO standard proposes Cyclic Redundancy Check, CRC, algorithm for protection of packet control data and payload. There are separate TX and RX parts. TX part calculate CRC on TX Packet and insert 16 bit word at the end of packet. RX part calculate CRC on incoming Packet, checks if CRC calculated and received CRC fields are matching, and report surrounding modules about it.

**Link layer.** Physical layer features such as packet acknowledge mechanism, packet delimiting, packet flow control are supported in this segment of Core. There is single module for TX and RX branch.

**Lane Front end.** Physical layer features such as 8B/10 encoding/decoding, Idle sequence generation/detection, Clock compensation sequence generation are supported in this segment of Core. There are separate TX and RX parts. Tx part output toward Serdes is 10bit code group, as well as RX part input from Serdes.
**HIP3300 Serial RapidIO Features:**
- Physical Coding Sub-layer (PCS)
- 8B/10B Encoding and Decoding support
- Physical Medium Attachment (PMA)
- Error management extensions
- Clock and Data Recovery
- Lane Synchronization
- CRC Generation and Checking
- Packet/Control Symbol Assembly and Deassembly
- Supports all RapidIO packet sizes
- Long control symbols
- Scrambler/Descrambler
- Idle2 sequence
- Idle2 CS
- RT Virtual channels
- CT Virtual channels

**Deliverables**
- Single or multi-use license
- Verilog RTL source code
- Comprehensive documentation package
- Functional specification
- Microarchitecture
- User guide

**HDL Design House Representatives**

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