V-by-One® PCS Tx IP Core (HIP 700_vby1_tx)

29.07.2018.

Design House
SoC Design and Verification Company

Overview

HDL Design House provides a set of IP cores for reuse along with IP core customization services to meet specific customer needs. Optimized for today's SoC designs, these IP cores are supported with full documentation, including architectural and micro-architectural specifications, synthesis scripts, detailed test plans, test case definitions and test bench descriptions.This IP core has been designed and verified using Cadence state-of-the-art EDA tools, methodology and recommanded design and verification flow.

The V-by-One Standard

The V-by-One standard was developed by Japan's THine Electronics, and defines a serial data transport link, which presents the following features:

Runs at speeds of up to 4Gbps per lane
Supports between 1 – 32 lanes
Uses data scrambling to reduce EMI signature
Targeted for low-power, high-speed digital video data transmission
Performs data alignment and synchronizations
Includes link monitoring functions
Allows for the transmission of 3D video
Features color depths of 18,24, 30 & 36 bits per pixel
Supports video refresh rates of 60, 120, 240 & 480 Hz
Supports a variety of video resolutions (HD, Full HD, Cinema Full HD, 4k x 2k)

Key Features:

- *Fully compatible with the V-by-One HS 1.4 standard release*
- *Includes the complete PCS functionality Supports a programmable number of data lanes (from 4 up to 32)*
- *Supports the generation of ALN training patterns.*
- *Designed to be used with Silicon Creations' 4-Lane, Multi-Protocol Serializer Hard IP Core Configured through APB slave interface*
- *Highly configurable*
  - *Number of data lanes*
  - *Lane rate*
  - *Scrambler enable*
  - *Inversion of video control signals*
  - *Lock filter enable*
- *Detects loss of synchronization automatically*
- *Contains a DFT interface and associated logic for digital scan test*
- *Features a power-down mode, used when the PCS is not active in the system*
- *Modular, completely synchronous designed*
- *Silicon proven*

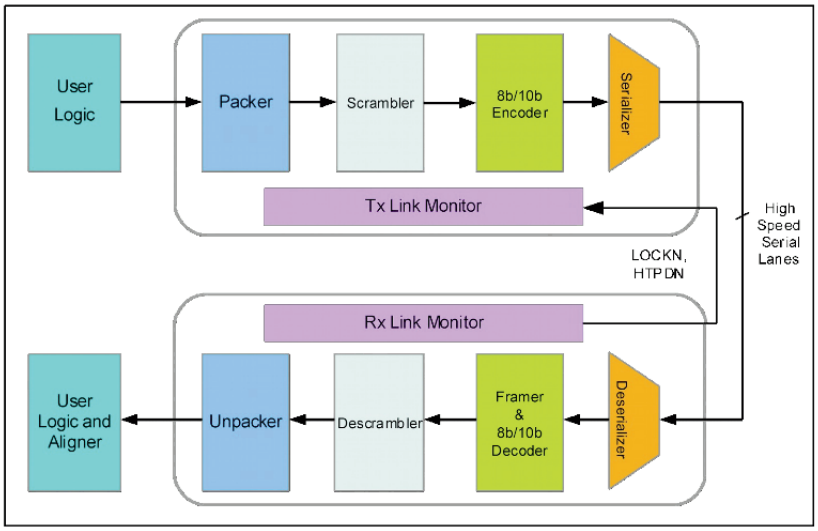

Figure1. Data Flow in V-by-One System

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Applications

- The main application space for the V-by-One controllers is in the video transport segment
- Automative infotainment systems
- Computer monitors
- Industrial camera-based systems
- Robotics – machine vision
- Flat panel displays
- Digital TV sets

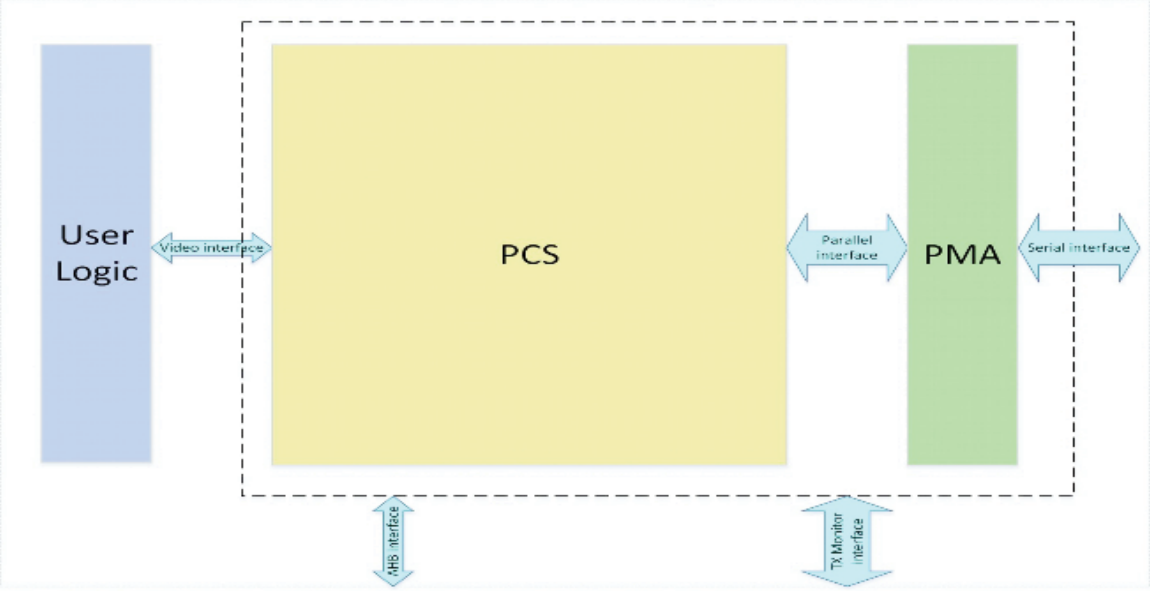

Figure2. The System Level Application of the HIP700 IP Core

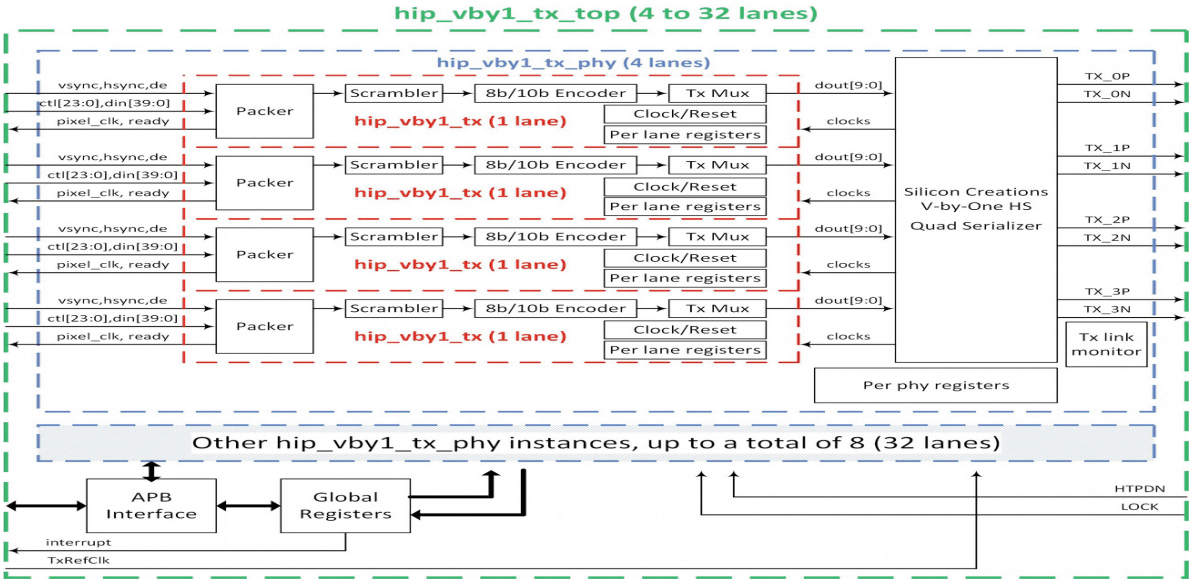

Figure3. HIP700 PHY Block Diagram

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Deliverables

- Marketing datasheet (pdf)
- Extended datasheet (pdf)
- Functional specification(pdf)
- Microarchitecture document (pdf)
- Synthesis scripts and reports (doc)
- STA scripts and reports(doc)note1
- DFT scripts and reports(doc)note2
- CDC scripts and reports(odc)
- Unencripted RTL files (Verilog source files)
- Verification & test plans (pdf)
- Verification environment (System Verilog source files)
- Coverage reports (doc)
- System integration guide (pdf)

Note1: Synthesis and STA scripts will be delivered as one or more script files for synthesis tool
Note2: DFT scripts may be integrated in synthesis and STA scripts

HDL Design House Representatives

For complete list of HDL Design House representatives visit following link:
http://www.hdl-dh.com/sales_rep.html

Contact Information

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